



CrossCom Safety IP Design Package

Overview

Functional safety related software and hardware require a certain safety integrity level. To achieve SIL3 typically 2 MCUs with mutual synchronization and monitoring are used (*1-out-of-2-Architecture*).

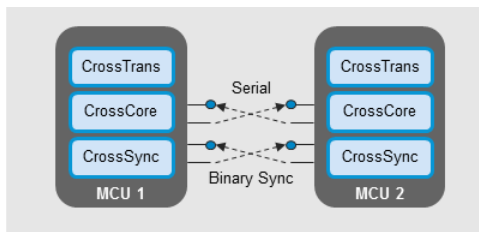


Fig. 1: Typical CrossCom Architecture

The CrossCom Safety IP Design Package is the central software component in such architecture.

Technical Description

This Design Package is the relevant component for exchanging data between two microcontrollers in a redundant SIL3 core architecture. It offers clear software interfaces, it is encapsulated and tested.

It mainly provides

- Timing synchronization of two microcontrollers for mutual monitoring
- Symmetric and asymmetric message exchange between two redundant microcontrollers for mutual monitoring
- Handling of data exchange for Safety Ethernet Communication with Black Channel technology

Your Benefits

- Design Package directly useable in SIL3 related projects
- Reduced development risk through reuse
- Saving on development by using proven architecture
- Cost and risk reduction of the project
- Shorter time-to-market through effort reduction
- Easier product certification due to IEC based documentation

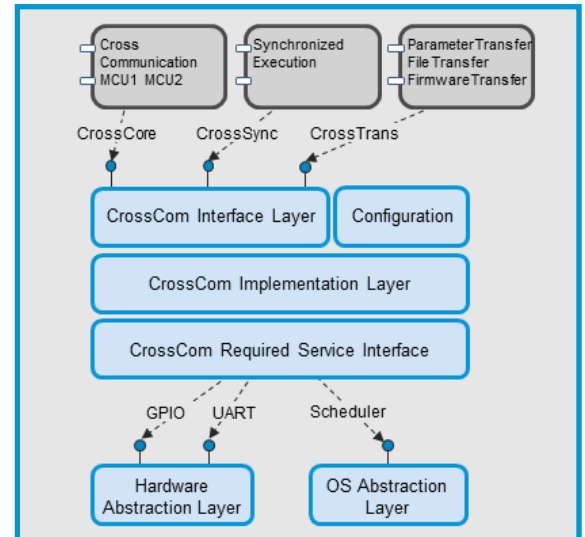


Fig. 2: CrossCom Layer Overview

Delivery Content

- SW design description (Polarion)
- Source code (IEC 61508 compliant, C99 MISRA-C 2012)
- Test documentation: test cases and test reports (Tessy)
- Code documentation (Doxygen)
- Static code analysis results (PC Lint)
- All documentation according to IEC 61508 standards

Software and hardware requirements

- Failure Handler (Interface)
- UART (Interface)
- GPIO (Interface)
- Opt. scheduler for asynchronous evaluation of messages
- Asynchronous communication interface needed (HW abstraction)
- Ring buffer for incoming message data
- Bulk data transfer for transmission
- 2 digital lines between microcontrollers
- Designed and optimized for STM 32-Bit microcontroller