



# IO-Link

## EMC Test Device for Masters

### Overview

The IO-Link Interface Specification V1.1.2 defines a test device (see Appendix G.2.2 Test of a Master) that must be connected to an IO-Link Master during the execution of EMC tests.

### Functional Description

The device generates an 8-bit random number which is read by the master. During the test, the master must return this random number to the device in the next IO-Link cycle.

The device checks whether it receives the correct random number, and if not, it increments an internal error counter. The error counter is also incremented if a checksum error or a parity error is detected on the device side.

The error count can be read by the master via an IO-Link parameter after the test. In addition, the error counter value is also displayed by a 7-segment indicator.

When an error is detected, the device generates a trigger signal at an optical output. A trigger box that converts the optical signal into a trigger pulse can be connected to the device. The trigger pulse supports developers in identifying possible issues on the master side.

The device can be configured to operate in one of the three COM speeds via DIP-Switches.



*IO-Link EMC Test Devices. Universal, smart, easy.*

### Features

- Device fully compliant with the IO-Link Interface Specification V1.1.2
- All three COM speeds are supported
- Internal Pseudo-Random-Number Generators
- Error counter for Parity, Checksum, Data and Time-out Errors
- 7-Segment Error Counter Display
- 7-Segment Device Status Display
- Error Counter accessible via IO-Link
- Optical Error Trigger Output

### Advantages

- No development effort for master manufacturers
- Faster time-to-market
- Identification of EMC issues

### Deliverables

- IO-Link EMC Test Device (with IODD)
- IO-Link Trigger hardware
- Optical link

